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[Title of the Invention] Control Circuit for DC/DC Converter and DC/DC Converter

[Inventor]

(Address) C/O FUJITSU VLSI LIMITED
1844-2, Kozoji-cho 2-chome, Kasugai-shi, Aichi

(Name) Kyuichi Takimoto

[Inventor]

(Address) C/O FUJITSU VLSI LIMITED
1844-2, Kozoji-cho 2-chome, Kasugai-shi, Aichi

(Name) Takashi Matsumoto

[Inventor]

(Address) C/O FUJITSU VLSI LIMITED
1844-2, Kozoji-cho 2-chome, Kasugai-shi, Aichi

(Name) Akira Haraguchi

[Applicant for Patent Application]

(Applicant Registration No.) 000005223

(Name) FUJITSU LIMITED

[Agent]

(Registration Number) 100068755

(Patent Attorney)

(Name) Hironori Onda

[Agent]

(Registration Number) 100105957

(Patent Attorney)

(Name) Makoto Onda

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[Title of the Document] Specification

[Title of the Invention] Control Circuit for DC/DC Converter and DC/DC Converter

[Scope of Claims]

[Claim 1] A control circuit for a DC/DC converter including a main switching element and a synchronous switching element, which are connected in series, and an externally connected element formed by connecting a smoothing circuit and a fly-back diode to a median point between the two switching elements, wherein the DC/DC converter outputs a first drive signal and a second drive signal to the main switching element and the synchronous switching element to alternately turn ON and OFF the two elements, the DC/DC converter control circuit being characterized by:

an idle period setting circuit for setting a synchronous rectification idle period in the drive signal provided to the main switching element and the synchronous switching element so that the two elements are not synchronously turned ON, wherein the idle period setting circuit substantially equalizes the pulse width of the drive signal provided to the main switching element and the pulse width so that the output voltage of the DC-DC converter becomes equal to a set voltage.

[Claim 2] The DC/DC converter according to claim 1, being characterized by:

an error amplification circuit for comparing a divided voltage of the output voltage with a reference voltage to generate an error signal;

a comparison circuit for comparing the error signal with a triangular wave signal to generate a pulse signal having a pulse width that is proportional to the voltage of the error signal; and

first and second output circuit for generating the first and second drive signals based on the pulse signal;

wherein the idle period setting circuit generates first and second control signals to set the synchronous rectification idle period in the first and second drive signals respectively provided to the main switching element and the synchronous switching element so that the two elements are not simultaneously turned ON;

the first output circuit generates a first drive signal provided to the main switching element based on the first control signal; and

the second output signal generates a second drive signal provided to the synchronous switching element based on the second control signal.

[Claim 3] The DC/DC converter control circuit according to claim 2, being characterized in that the idle period setting circuit delays the rising edge and the falling edge of the pulse signal to generate the first control signal.

[Claim 4] The DC/DC converter control circuit according to claim 2 or 3, being characterized in that the idle period setting circuit synthesizes the delay signal, which delays the rising edge and the falling edge of the first control signal, with the pulse signal to generate the second control signal.

[Claim 5] The DC/DC converter control circuit according to claim 2, being characterized in that the idle period setting circuit includes:

a first delay circuit for delaying the rising edge and the falling edge of the pulse signal to generate the first control signal;

a second delay circuit for inputting the pulse signal or the first control signal and delaying the rising edge and the falling edge of the input signal to generate a delay

signal; and

a synthesizing circuit for logically synthesizing the pulse signal and the delay circuit to generate the second control signal.

[Claim 6] The DC/DC converter control circuit according to claim 5, being characterized in that the first and second delay circuits delay the input signal with a plurality of series-connected inverter circuits.

[Claim 7] The DC/DC converter control circuit according to claim 5, being characterized in that the first and second delay circuits delay the input signal with a time constant of a resistor and a capacitor.

[Claim 8] A DC/DC converter including a main switching element and a synchronous switching element, which are connected in series, and an externally connected element formed by connecting a smoothing circuit and a fly-back diode to a median point between the two switching elements, and a control circuit for outputting a first drive signal and a second drive signal to the main switching element and the synchronous switching element to alternately turn ON and OFF the two elements, the DC/DC converter being characterized in that:

the control circuit includes an idle period setting circuit for setting a synchronous rectification idle period in the drive signal provided to the main switching element and the synchronous switching element so that the two elements are not synchronously turned ON;

wherein the idle period setting circuit substantially equalizes the pulse width of the drive signal provided to the main switching element and the pulse width so that the output voltage of the DC-DC converter becomes equal to a set voltage.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a DC/DC converter, and, more particularly, to a synchronous rectification-type DC/DC converter used as a power supply for a variety of electronic devices and a control circuit for the converter.

[0002]

In recent years, the operation frequency of CPUs and the like used in various electronic devices has increased speed. This has increased the power supply current. Thus, the power has been increased for a synchronous rectification type DC/DC converter used as a power supply for CPUs or the like. A DC/DC converter alternately turns ON and OFF a main switching element and a synchronous switching element, which are connected in series, to supply a load with constant voltage. By simultaneously turning ON the two switching elements, through current flows and increases the consumed current. To prevent the through current, a synchronous rectification idle period must be set to simultaneously turn OFF the two switching elements.

[0003]

[Prior Art]

Fig. 9 shows an example of a conventional sDC-DC converter. The DC/DC converter 1 includes a control circuit 2 formed on a single semiconductor integrated circuit substrate and a plurality of elements mounted externally.

[0004]

A first drive signal SG1 of the control circuit 2 is supplied to the gate of the main switching element 3, which is an enhancement-type N-channel MOS transistor. The switching element 3 operates as a main switch for driving a load. The first drive signal SG1 is applied to the gate of the switching element 3. The drain of the switching element

3 is supplied with a supply voltage Ve from a battery, while the source of the switching element 3 is connected to the synchronous switching element 4.

[0005]

The synchronous switching element 4 is an enhancement-type N-channel MOS transistor and has a drain connected to the source of the main switching element 3. The gate of the synchronous switching element 4 is supplied with a second drive signal SG2 of the control circuit 2, while the source thereof is connected to the ground GND.

[0006]

The source of the main switching element 3 is connected via a choke coil 5, which forms a smoothing circuit, to an output terminal To. The source of the main siwthcing element 3 is connected to the cathode of a fly-back diode 6. The anode of the diode 6 is connected to the ground GND.

[0007]

The synchronous switching element 4 operates when the DC/DC converter 1 is flying back, thus reducing loss at the fly-back diode 6.

The output terminal To is connected via the smoothing capacitor 7 to the ground GND. The output terminal To is connected to the load of a control unit such as a CPU (not shown). The output terminal To outputs voltage Vo. The output voltage Vo is divided by the resistors 8 and 9, and a divided voltage V2 is fed back to the control circuit 2.

[0008]

The control circuit 2 includes an error amplification circuit 11, a PWM comparison circuit 12, a triangular wave oscillation circuit 13, an idle period setting circuit 14, and first and second output circuits 15 and 16.

The error amplification circuit 11 receives the divided voltage V2 with an inverting input terminal and a reference

voltage Vr (set voltage) from a reference power supply E1 with a non-inverting input terminal.

[0009]

The error amplification circuit 11 compares the divided voltage V2 with the reference voltage Vr serving as a set voltage and amplifies a differential voltage between the two, thus generating an error signal S1, which is provided to the PWM comparison circuit 12 in the next stage.

[0010]

The PWM comparison circuit 12 compares the error signal S1 supplied to the non-inverting input terminal from the error amplification circuit 11 and a triangular wave signal S2 supplied to the inverting input terminal from the triangular wave oscillation circuit 13.

The PWM comparison circuit 12 compares the levels of the error signal S1 and the triangular wave signal S2 to generate a pulse signal S3 having a low (L) level in a period for which the triangular wave signal S2 is higher in level than the error signal S1 and the pulse signal S3 having a high (H) level in a period opposite to it. The pulse signal S3 is provided to the idle period setting circuit 14.

[0011]

Based on the pulse signal S3, the idle period setting circuit 14 generates first and second control signals S4 and S5 such that the main switching element 3 and the synchronous switching element 4 are turned ON and OFF substantially complementarily and also such that they are not turned ON simultaneously (this period is referred to as a synchronous rectification idle period (hereinafter called idle period)). The idle period is set to prevent the system from being destroyed by an excessive through current which would flow through the switching elements 3 and 4 if the

main switching elements 3 and 4 were turned ON simultaneously.

[0012]

The first output circuit 15 amplifies the first control signal S4 supplied from the idle period setting circuit 14, to generate a first drive signal SG1 supplied to the main switching element 3. The second output circuit 16 amplifies the second control signal S5 supplied from the idle period setting circuit 14, to generate a second drive signal SG2 supplied to the synchronous switching element 4.

[0013]

Fig. 10 is a circuit diagram of the convention idle period setting circuit 14.

The idle period setting circuit 14 includes inverter circuits 21 to 25, transistors T1 and T2, power supplies 26 and 27, and capacitors C1 and C2.

[0014]

The pulse signal S3 is supplied to the inverter circuit 21, which in turn supplies an inverted signal of the pulse signal S3 to the gate of the N-channel MOS transistor T1. The source of the transistor T1, which is an N-channel MOS transistor, is connected to the ground GND and the drain thereof is connected to the current source 26.

[0015]

A node between the transistor T1 and the current source 26 is connected to the first terminal of the capacitor C1, and the second terminal of the capacitor C1 is connected to the ground GND. Further. the first terminal of the capacitor C1 is connected to the input terminal of the inverter circuit 22. The output terminal of the inverter circuit 22 is connected to the input terminal of the inverter circuit 23, which outputs the first control signal S4.

[0016]

As shown in Fig. 11, when the pulse signal S3 rises, an input signal S6 of the inverter circuit 22 also rises in accordance with a current I1 from the current source 26 and a capacitance of the capacitor C1. Activation of the transistor T1 causes the input signal S6 to fall rapidly. When the voltage of the input signal S6 exceeds a threshold voltage Vth of the inverter circuit 22, the inverter circuit 22 inverts the input signal S6. Therefore, the first control signal S4 rises as delayed with respect to the rising timing of the pulse signal S3 by time td1 which corresponds to charging time of the capacitor C1 and falls substantially at the same time as the pulse signal S3 falls. The delay time td1 is obtained by:

$$td1 = Vth*C1/I1$$

[0017]

The pulse signal S3 is supplied to the gate of the N-channel MOS transistor T2. The source of the transistor T1 is connected to the ground GND and the drain thereof is connected to the current source 27.

[0018]

A node between the transistor T2 and the current source 27 is connected to the first terminal of the capacitor C2, and the second terminal of the capacitor C2 is connected to the ground GND via the capacitor C2. Further, the first terminal of the capacitor C2 is connected to the input terminal of the inverter circuit 24. The output terminal of the inverter circuit 24 is connected to the input terminal of the inverter circuit 25. The inverter circuit 25 outputs the second control signal S5.

[0019]

As shown in Fig. 3, in response to the pulse signal S3 the transistor T2 is turned ON, thus causing an input signal S7 of the inverter circuit 24 to fall rapidly. The rising

edge of the pulse signal S3 has a rising waveform that is in accordance with the current amount I2 of the current source 27 and the capacitance of the capacitor C2. Subsequently, when the voltage of the input signal S7 exceeds a threshold voltage Vth of the inverter circuit 24, the inverter circuit 24 inverts the input signal S7. Therefore, the second control signal S5 falls substantially at the same time as the pulse signal S3 rises and rises as delayed with respect to the rising timing of the pulse signal S3 by delay time td2 which corresponds to charging time of the capacitor C2. The delay time td2 is obtained by:

$$td2 = Vth*C2/I2$$

[0020]

[Problems That Are To Be Solved By the Invention]

It is required that the DC/DC converter 1 operates on a low supply voltage in order to reduce power consumption. The idle period setting circuit 14, however, generates the first control signal S4 which has a pulse width smaller than that of the pulse signal S3 by the delay time td1. Accordingly, as shown in Fig. 12, an ON-duty ratio of the first control signal S4 with respect to the voltage of the error signal S1 becomes smaller than that of ideal characteristics. Therefore, it is impossible to set the duty ratio of the first control signal S4, or the first drive signal SG1, to a high value, for example, a value in the vicinity of 100%. For this reason, in the conventional DC/DC converter 1, it is difficult to lower the supply voltage to reduce the power consumption.

[0021]

Accordingly, the present invention has been made to solve the above problem and its object is to provide a DC/DC converter control circuit and DC/DC converter for improving the ON duty characteristic of the main switching element.

[0022]

[Means for Solving the Problems]

To achieve the above object, the invention of claim 1 is control circuit for a DC/DC converter including a main switching element and a synchronous switching element, which are connected in series, and an externally connected element formed by connecting a smoothing circuit and a fly-back diode to a median point between the two switching elements, wherein the DC/DC converter outputs a first drive signal and a second drive signal to the main switching element and the synchronous switching element to alternately turn ON and OFF the two elements. The DC/DC converter control circuit includes an idle period setting circuit for setting a synchronous rectification idle period in the drive signal provided to the main switching element and the synchronous switching element so that the two elements are not synchronously turned ON, wherein the idle period setting circuit substantially equalizes the pulse width of the drive signal provided to the main switching element and the pulse width so that the output voltage of the DC-DC converter becomes equal to a set voltage. Accordingly, the main switching element is turned ON and OFF by a drive signal having a pulse width with a duty set in accordance with the output voltage.

[0023]

The invention of claim 2 includes an error amplification circuit for comparing a divided voltage of the output voltage with a reference voltage to generate an error signal, a comparison circuit for comparing the error signal with a triangular wave signal to generate a pulse signal having a pulse width that is proportional to the voltage of the error signal, and first and second output circuit for generating the first and second drive signals based on the

pulse signal. The idle period setting circuit generates first and second control signals to set the synchronous rectification idle period in the first and second drive signals respectively provided to the main switching element and the synchronous switching element so that the two elements are not simultaneously turned ON. The first output circuit generates a first drive signal provided to the main switching element based on the first control signal. The second output signal generates a second drive signal provided to the synchronous switching element based on the second control signal. Accordingly, the main switching element is turned ON and OFF by a drive signal having a pulse width with a duty set in accordance with the output voltage.

[0024]

In the invention of claim 3, the idle period setting circuit delays the rising edge and the falling edge of the pulse signal to generate the first control signal. Accordingly, the main switching element generates a drive signal having a pulse width with a duty set in accordance with the output voltage.

[0025]

In the invention of claim 4, the idle period setting circuit synthesizes the delay signal, which delays the rising edge and the falling edge of the first control signal, with the pulse signal to generate the second control signal. This ensures that the synchronous rectification idle period of the main switching element and the synchronous switching element are set.

[0026]

In the invention of claim 5, the idle period setting circuit includes a first delay circuit for delaying the rising edge and the falling edge of the pulse signal to

generate the first control signal, a second delay circuit for inputting the pulse signal or the first control signal and delaying the rising edge and the falling edge of the input signal to generate a delay signal, and a synthesizing circuit for logically synthesizing the pulse signal and the delay circuit to generate the second control signal.

[0027]

In the invention of claim 6, the first and second delay circuits delay the input signal with a plurality of series-connected inverter circuits. The delay time of the input signal corresponds to the synchronous rectification idle time. Accordingly, the synchronous rectification idle time is easily set.

[0028]

In the invention of claim 7, the first and second delay circuits delay the input signal with a time constant of a resistor and a capacitor. The delay time of the input signal corresponds to the synchronous rectification idle time. Accordingly, the synchronous rectification idle time is easily set.

[0029]

The invention of claim 8 is a DC/DC converter including a main switching element and a synchronous switching element, which are connected in series, and an externally connected element formed by connecting a smoothing circuit and a fly-back diode to a median point between the two switching elements, and a control circuit for outputting a first drive signal and a second drive signal to the main switching element and the synchronous switching element to alternately turn ON and OFF the two elements. In the DC/DC converter, the control circuit includes an idle period setting circuit for setting a synchronous rectification idle period in the drive signal provided to the main switching

element and the synchronous switching element so that the two elements are not synchronously turned ON. The idle period setting circuit substantially equalizes the pulse width of the drive signal provided to the main switching element and the pulse width so that the output voltage of the DC-DC converter becomes equal to a set voltage. Accordingly, the main switching element is turned ON and OFF by a drive signal having a pulse width with a duty set in accordance with the output voltage.

[0030]

[Embodiment of the Invention]

An embodiment of the present invention will now be described with reference to Figs. 1 to 5.

For the sake of brevity, parts that are like to those of the prior art will be denoted with the same reference numbers and will not be described.

[0031]

Fig. 1 is a block circuit diagram of a DC/DC converter.

A DC/DC converter 31 includes a control circuit 32 formed on a single semiconductor integrated circuit substrate and seven elements externally mounted, that is, a main switching element 3, a synchronous switching element 4, a choke coil 5, a fly-back diode 6, a smoothing capacitor 7, and resistors 8 and 9. The choke coil 5 and the smoothing capacitor 7 constitute a smoothing circuit.

[0032]

The resistors 8 and 9 divide an output voltage Vo at an output terminal To, to supply a divided voltage V2 to the control circuit 32. Based on the divided voltage V2, the control circuit 32 generates a first drive signal SG11 supplied to the main switching element 3 and a second drive signal SG12 supplied to the synchronous switching element 4.

[0033]

The control circuit 32 includes an error amplification circuit 11, a PWM comparison circuit 12, a triangular wave oscillation circuit 13, an idle period setting circuit 34, and the first and second output circuits 15 and 16.

The error amplification circuit 11 receives the divided voltage V2 with the inverting input terminal and a reference voltage Vr from a reference power supply E1 with the non-inverting input terminal.

[0034]

The error amplification circuit 11 compares the divided voltage V2 and the reference voltage Vr and amplifies a differential voltage between the two, thus generating an error signal S1, which is provided to the PWM comparison circuit 12 in the next stage.

The PWM comparison circuit 12 receives the error signal S1 supplied to the non-inverting input terminal and the triangular wave signal S2 supplied to the inverting input terminal from the triangular wave oscillation circuit 13.

[0035]

The PWM comparison circuit 12 compares the levels of error signal S1 and the triangular wave signal S2 to generate a pulse signal S3 having an L level in a period for which a triangular wave signal S2 is higher in level than the error signal S1 and the pulse signal S3 having an H level in a period opposite to it.

[0036]

The idle period setting circuit 34 receives the pulse signal S3 from the PWM comparison circuit 12 and generates a first control signal S14 which has substantially the same pulse width as that of the pulse signal S3. Furthermore, based on the pulse signal S3 and the first control signal S14, the idle period setting circuit 34 generates a second control signal S15 such that the main switching element 3

and the synchronous switching element 4 are turned ON and OFF substantially complementarily and also such that they are not turned ON simultaneously (that is, the switching elements 3 and 4 are turned ON and OFF alternately at different timings). An idle period in which the switching elements 3 and 4 are not turned ON simultaneously is set in order to prevent the system from being destroyed by an excessive current which would flow if the switching elements 3 and 4 were turned ON simultaneously.

[0037]

The first output circuit 15 amplifies the first control signal S14 supplied from the idle period setting circuit 34 and generates the first drive signal SG11 supplied to the main switching element 3. The second output circuit 16 amplifies the second control signal S15 supplied from the idle period setting circuit 34 and generates a second drive signal SG12 supplied to the synchronous switching element 4.

[0038]

Fig. 2 is a block circuit diagram illustrating the principle of the idle period setting circuit 34.

The idle period setting circuit 34 includes first and second delay circuits 35 and 36 and a synthesis circuit 37.

[0039]

The first delay circuit 35 delays the pulse signal S3 by a predetermined delay time td1 to generate the first control signal S14 having substantially the same pulse width as that of the pulse signal S3 as shown in Fig. 3. The first control signal S14 is output to the second delay circuit 36.

[0040]

The second delay circuit 36 receives the first control signal S14 from the first delay circuit 35 and delays the first control signal S14 by a predetermined delay time td2 to generate a delayed signal S16 having substantially the

same pulse width as that of the first control signal S14 (pulse signal S3) as shown in Fig. 3. The delay signal S16 is output to the synthesis circuit 37.

[0041]

The synthesis circuit 37 receives the pulse signal S3 and the delayed signal S16 and, as shown in Fig. 3, logically synthesizes the pulse signal S3 with the delayed signal S16 to generate the second control signal S15 such that the main switching element 3 and the synchronous switching element 4 are turned ON and OFF substantially complementarily and also such that these two switching elements 3 and 4 are not turned ON simultaneously (period referred to as idle period).

[0042]

In such a manner, the idle period setting circuit 34 generates the first control signal S14 having substantially the same pulse width as that of the pulse signal S3. Therefore, an ON-duty ratio of the first control signal S14 with respect to a voltage of the error signal S1, which is supplied to the PWM comparison circuit 12, is substantially consistent with that of the ideal characteristics. It is thus possible to set the duty ratio of the first control signal S14 (that is, first drive signal SG11) in the vicinity of 100%, for example.

[0043]

Fig. 4 is a circuit diagram showing an example of the idle period setting circuit 34.

The idle period setting circuit 34 includes first and second delay circuits 35 and 36 and the synthesis circuit 37. The first delay circuit 35 of the idle period setting circuit 34 includes a plurality (m number) of serially connected inverter circuits in the present embodiment and outputs a signal S3 delayed by the delay time td1 which is

determined by m which indicates the number of the inverter circuits. The second delay circuit 36 includes a plurality (n number) of serially connected inverter circuits in the present embodiment and outputs a signal delayed by the delay time td2 which is determined by n which indicates the number of the inverter circuits. In the present embodiment, the synthesis circuit 37 is a NOR circuit and performs a neither-nor operation on the pulse signal S3 and the delay signal S16 to generate the second control signal S15. In accordance with the logic of the input pulse signal S3 and the delay signal S16, the synthesis circuit 37 may be formed by an OR circuit or an inverter circuit arranged at an input side.

[0044]

The idle period setting circuit 34 includes inverter circuits 41 to 44 which are provided so that a logical level of the pulse signal S3 may match that of the first and second control signals S14 and S15 in accordance with the circuit configurations of the first and second delay circuit 35 and 36 and the synthesis circuit 37.

[0045]

For example, if an even number of the inverters are included in the first delay circuit 35, a path, to which the pulse signal S3 is supplied and from which the first control signal S14 is output, is provided with an even number of the inverter circuits. Then, the inverter circuits are inserted in accordance with how the first and second delay circuits 35 and 36 are interconnected.

[0046]

As described above, the idle period setting circuit 34 generates the first control signal S14 having a pulse width that is substantially the same as the pulse signal S3 input from the PWM comparison circuit 12 of Fig. 1. Accordingly,

as shown in Fig. 5, the setting of the ON duty ratio of the first control signal S14 for the voltage of the error signal S1 input to the PWM comparison circuit 12 (refer to Fig. 1) is substantially equalized with the ideal characteristics. This enables the duty of the first control signal S14, and thus, the first drive signal SG11, to be high thereby allowing a setting of substantially 100 percent. Further, the power supply voltage may be lowered.

[0047]

The DC/DC converter 31 of the present embodiment has the following advantages.

(1) The idle period setting circuit 34 delays the pulse signal S3 supplied from the PWM comparison circuit 12 and generates the first control signal S14 which has substantially the same pulse width as that of the pulse signal S3. The main switching element 3 is turned ON and OFF by the first drive signal SG11 which has a pulse width that corresponds to an ideal duty ratio which is set in accordance with the output voltage Vo. As a result, the duty ratio of the first drive signal SG11 can be set to 100%.

[0048]

(2) The synthesis circuit 37 of the idle period setting circuit 34 logically synthesizes the pulse signal S3 and the delayed signal S16 of the first control signal S14 and generates the second control signal S15. The synchronous switching element 4 is securely maintained OFF while the main switching element 3 is ON. Therefore, the idle period is securely set. That is, the idle period is easily set.

[0049]

The present embodiment may be modified as described below.

The idle period setting circuit 34 may be replaced by an idle period setting circuit 50 such as shown in Fig. 6.

Fig. 7 is a waveforms chart of the idle period setting circuit 50.

[0050]

The idle period setting circuit 50 includes first and second delay circuits 51 and 52, a synthesis circuit 53, and inverter circuits 54 to 58. The first delay circuit 51 is an integrating circuit which includes a resistor 61 connected between the inverters 55 and 56, and a capacitor 62 connected between a node, between the resistor 61 and the inverter 56, and the ground. The integrating circuit generates an output signal whose through rate corresponding to the rising and falling timings of an input signal is delayed by a time constant, which output signal in turn delays the rising and falling timings of an output signal of the next-stage inverter circuit 56. In such a manner, the inverter circuit 56 generates a first control signal S23 which is delayed with respect to the pulse signal S3 by the delay time td1 and which has substantially the same pulse width as that of the pulse signal S3. The delay time td1 is determined by a resistance value R2 of the resistor 61, a capacitance value C2 of the capacitor 62, and a threshold value Vth1 of the inverter circuit 56 as follows:

$$td1 = C2 \times R2 \times \ln (Vth1)$$

[0051]

In the same manner, the second delay circuit 52 is an integrating circuit which includes a resistor 63 and a capacitor 64. The integrating circuit generates an output signal whose through rate corresponding to the rising and falling timings of an input signal is delayed by a time constant, which output signal in turn delays the rising and falling timings of an output signal of the next-stage inverter circuit 58. In such a manner, the inverter circuit 58 generates a delayed signal S25 which is delayed with

respect to a first control signal S23 by the delay time td2 and which has substantially the same pulse width as that of the pulse signal S3. The delay time td2 is determined by a resistance value R3 of the resistor 63, a capacitance value C3 of the capacitor 64, and a threshold value Vth2 of the inverter circuit 56 as follows:

$$td2 = C3 \times R3 \times \ln (Vth2)$$

[0052]

The synthesis circuit 53 is a NOR circuit which performs a neither-nor operation on the pulse signal S3 and the delayed signal S25 and generates the second control signal S26.

The first output circuit 15 receives the first control signal S23 and generates the first drive signal SG11, while the second output circuit 16 receives the second control signal 26 and generates the second drive signal SG12.

[0053]

The inverter circuits of the above embodiment may be formed as shown in Figs. 8(a) to 8(c).

The inverter circuit 71 of Fig. 18(a) includes a resistor 72 and an NPN transistor 73. The inverter circuit 74 of Fig. 8(b) includes a current source 75 and an NPN transistor 76. If these inverter circuits 71 and 74 are applied to the inverter circuits 54 to 58 and the synthesis circuit 53 of the idle period setting circuit 50 of Fig. 6, the inverter circuits 54 to 58 and the synthesis circuit 53 can be formed by the same process as that for the first and second delay circuits 51 and 52.

[0054]

The inverter circuit 77 of Fig. 8(c) is a CMOS inverter circuit which is comprised of a P-channel MOS transistor 78 and an N-channel MOS transistor 79. If this inverter circuit 77 is applied to the idle period setting circuits 34 and 50,

power consumption can be reduced.

[0055]

In the above embodiment, the configuration of the control circuit 32 may be changed.

The switching elements 3 and 4 and the voltage dividing resistors 8 and 9 may be formed together with the control circuit 32 on a single semiconductor integrated circuit substrate.

[0056]

[Effect of the Invention]

As described in detail above, the present invention provides a DC/DC converter control circuit and a DC/DC converter that improves the ON duty characteristic of the main switching element.

[Brief Description of the Drawings]

[Fig. 1] Block diagram of a DC/DC converter.

[Fig. 2] Block diagram of an idle period setting circuit.

[Fig. 3] Operating waveform diagram of the idle period setting circuit.

[Fig. 4] Circuit diagram of the idle period setting circuit.

[Fig. 5] Graph for showing an ON-duty ratio characteristic.

[Fig. 6] Circuit diagram of an alternative example of an idle period setting circuit.

[Fig. 7] Operating waveform diagram of the idle period setting circuit

[Fig. 8] (a) to 8(c) are circuit diagrams of inverter circuits.

[Fig. 9] Block diagram of a conventional DC/DC converter.

[Fig. 10] Circuit diagram of an idle period setting

circuit of the conventional DC/DC converter.

[Fig. 11] Operating waveform diagram of the idle period setting circuit.

[Fig. 12] Graph for showing an ON-duty ratio characteristic of the prior art example.

[Description of the Reference Numbers]

3 main switching element

4 synchronous switching element

6 fly-back diode

11 error amplification circuit

12 PWM comparison circuit

15 first output circuit

16 second output circuit

32 control circuit

34, 50 idle period setting circuit

35, 51 first delay circuit

36, 52 second delay circuit

37, 53 synthesis circuit

SG11, SG12 first and second drive signals

S1 error signal

S2 triangular wave signal

S3 pulse signal

S14, S23 first control signal

S15, S26 second control signal

S16, S25 delay signal

Vo output voltage

Vr set voltage

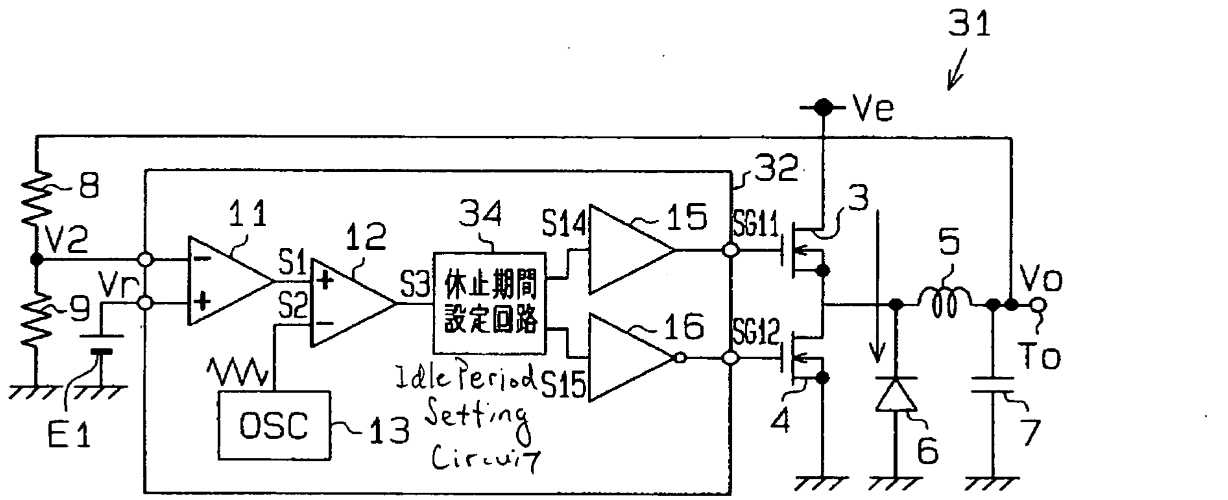
V2 divided voltage

【書類名】　図面　[Title of the Documents] Drawings

【図１】 [Fig. 1]

Block Circuit Diagram of DC/DC Converter

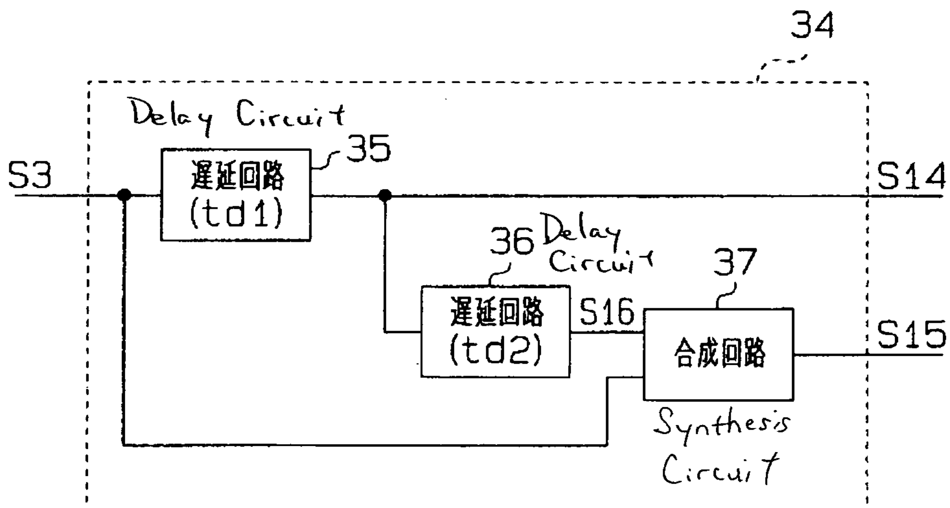
DC/DCコンバータのブロック回路図



【図２】[Fig. 2]

Block Circuit Diagram of Idle Period Setting Circuit

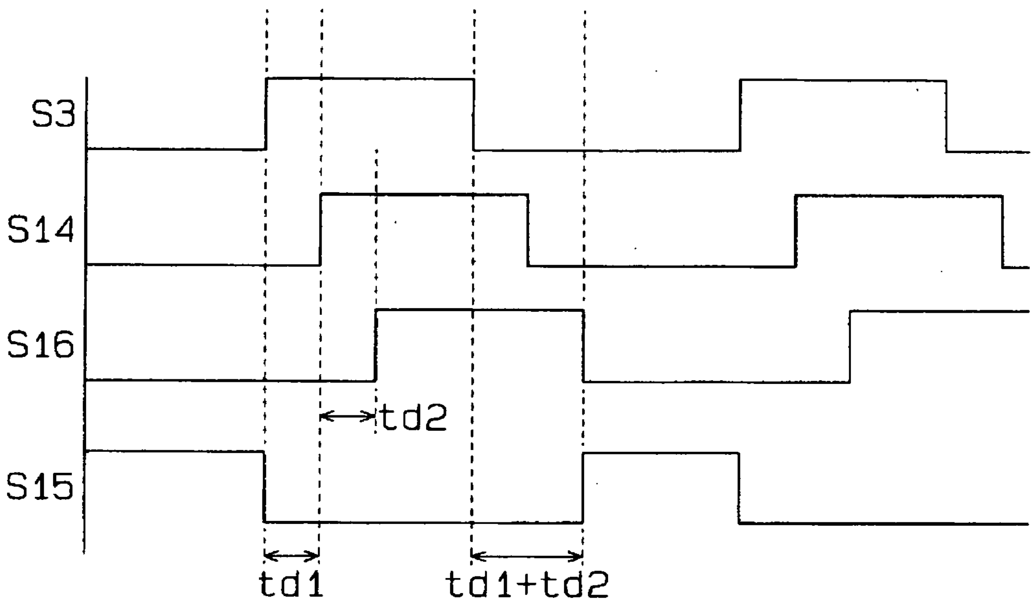
休止期間設定回路のブロック回路図



【図３】[Fig.3]

Operational Waveform Diagram of Idle Period Setting Circuit

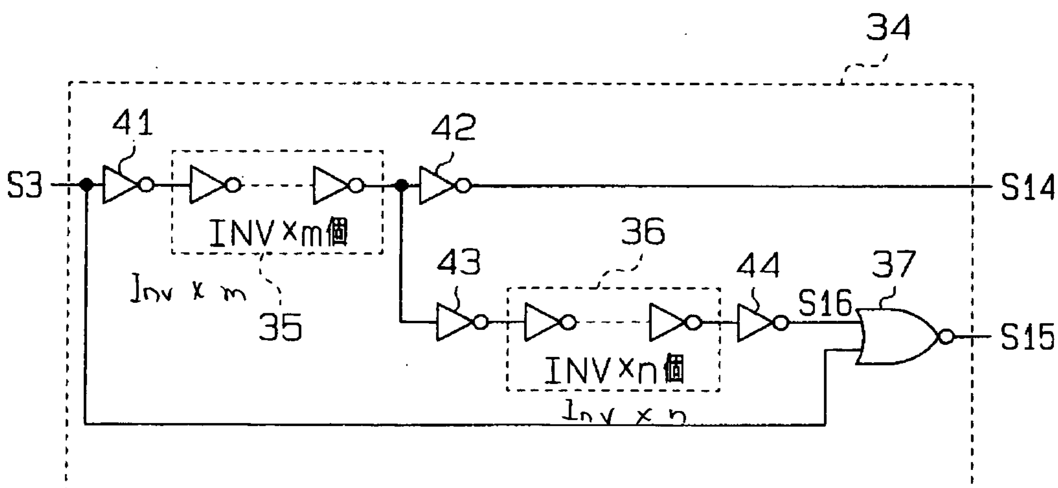
休止期間設定回路の動作波形図



【図４】[Fig.4]

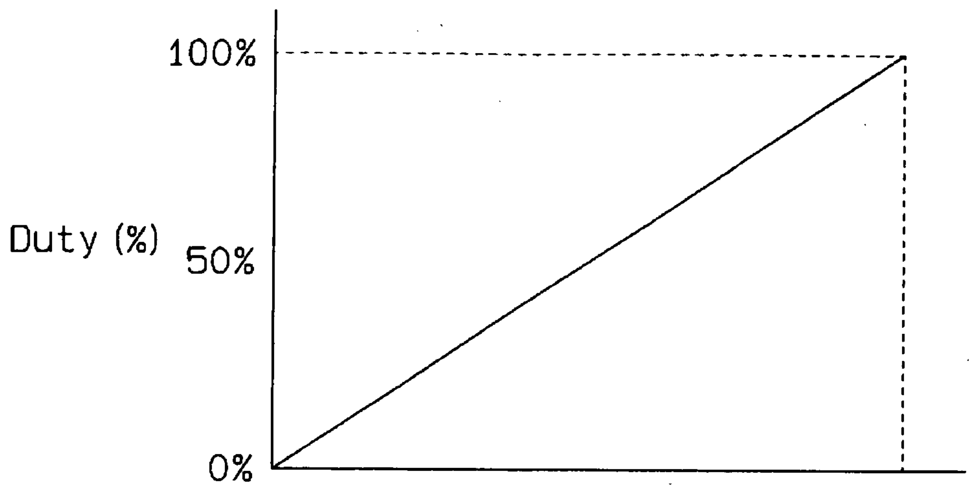
Circuit Diagram of Idle Period Setting Circuit

休止期間設定回路の回路図



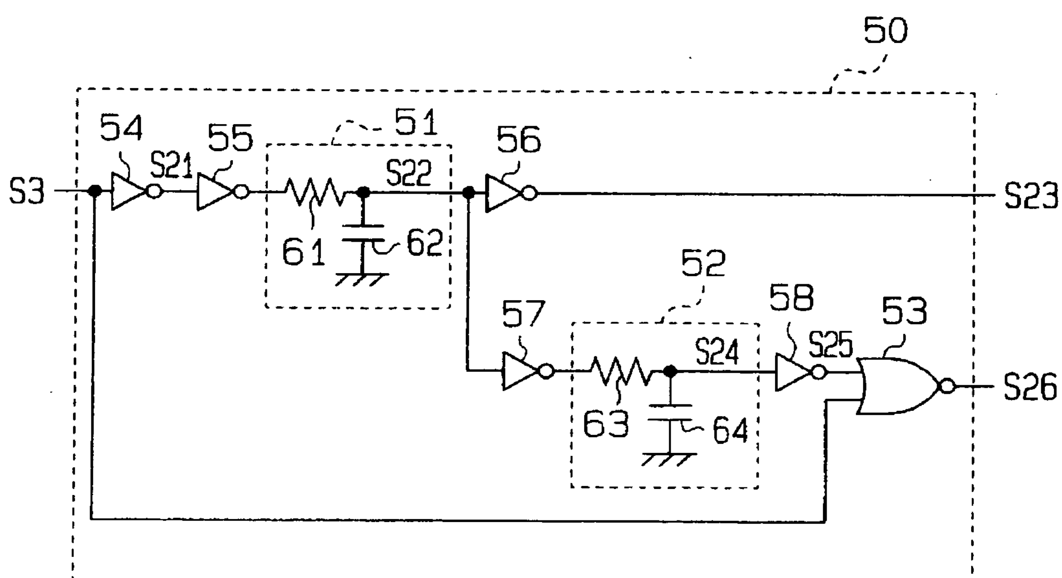
【図5】 [Fig. 5]

ON Duty Characteristic Diagram
オン・デューティ特性の説明図



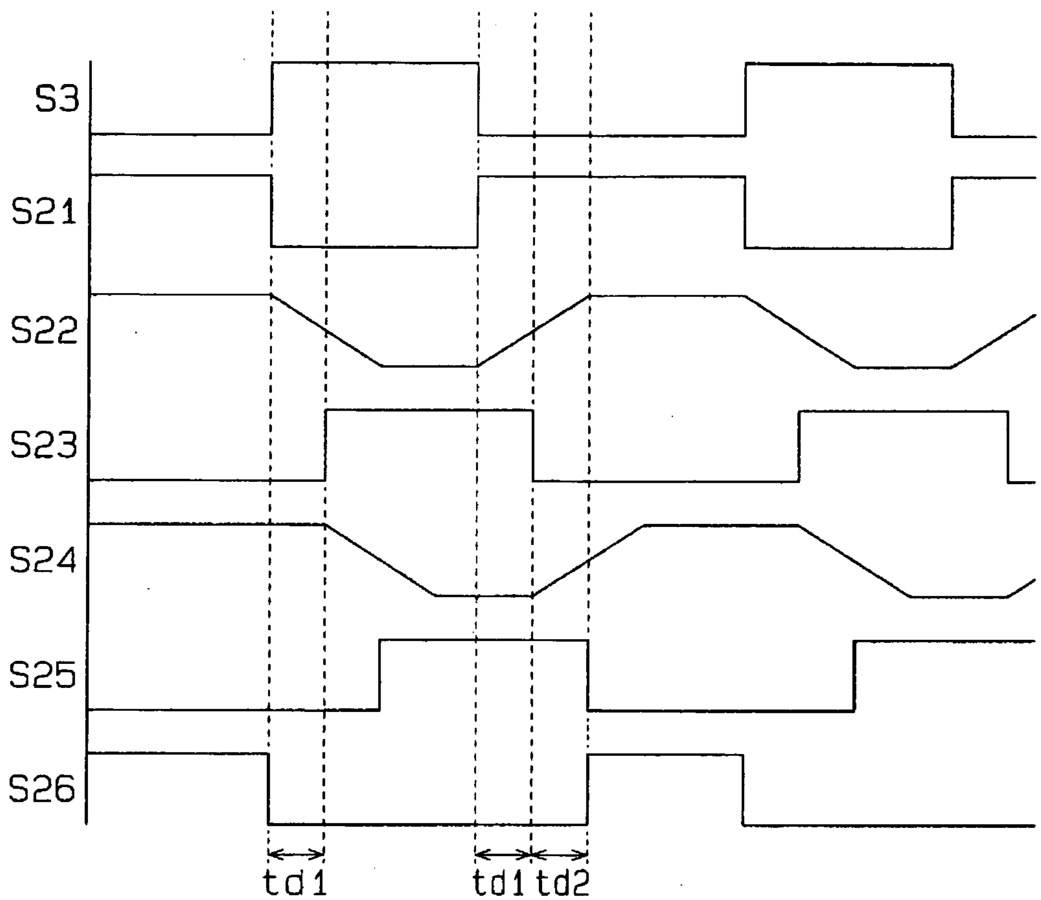
【図6】 [Fig. 6]

Circuit Diagram of Further Idle Period Setting Circuit
別の休止期間設定回路の回路図



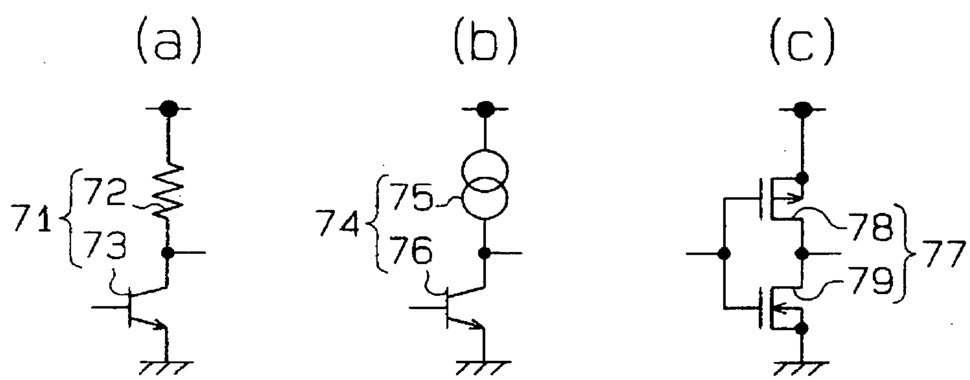
【図7】[Fig. 7]

Operational Waveform Diagram of Further Idle Period Setting Circuit
別の休止期間設定回路の動作波形図



【図8】[Fig. 8]

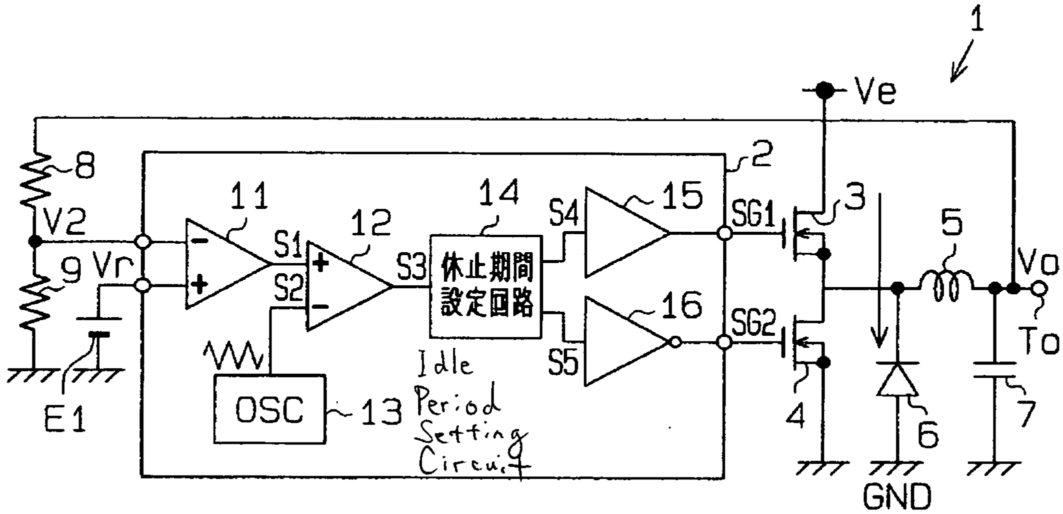
Diagrams Showing Circuit Examples of Inverter Circuits
インバータ回路の回路例を示す説明図



【図9】 [Fig.9]

Block Circuit Diagram of Prior Art DC/DC Converter

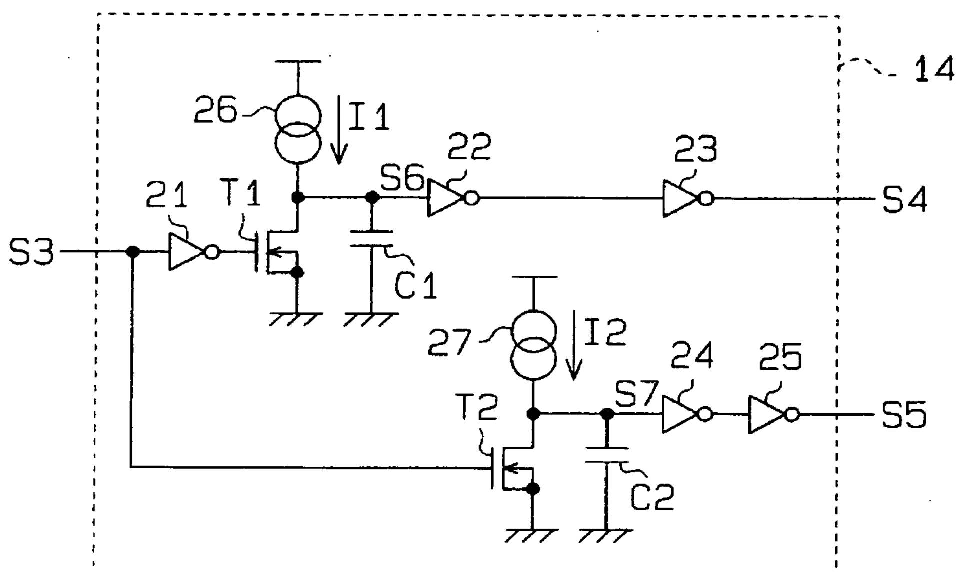
従来のDC/DCコンバータのブロック回路図



【図10】 [Fig.10]

Circuit Diagram of Prior Art Idle Period Setting Circuit

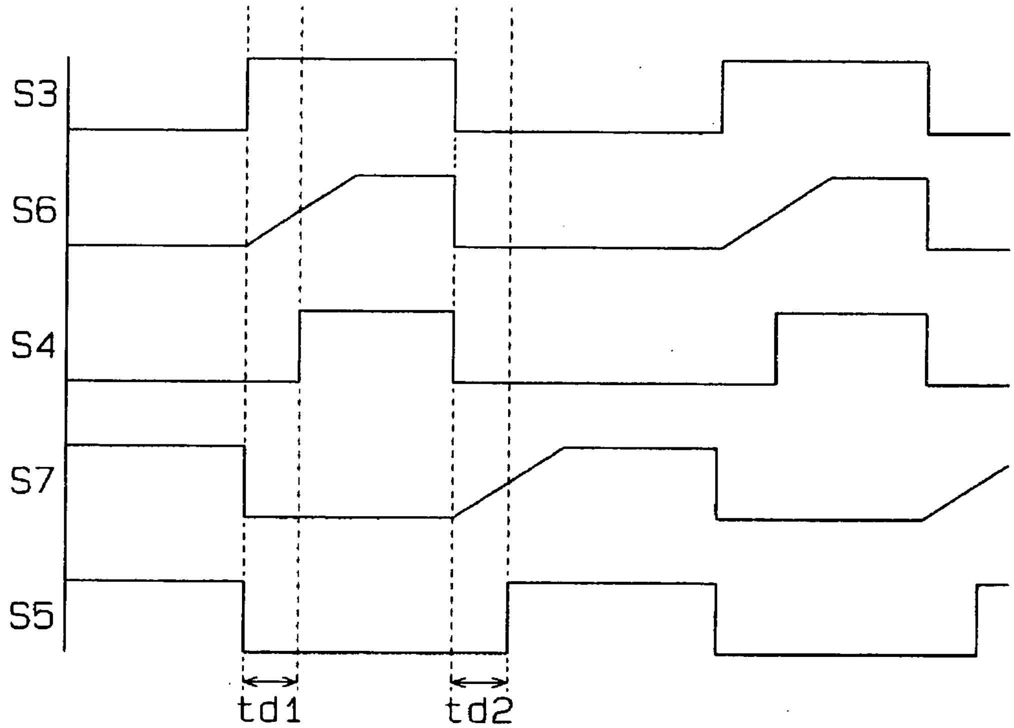
従来の休止期間設定回路の回路図



【図１１】[Fig.11]

Operational Waveform Diagram of Prior Art Idle Period Setting Circuit

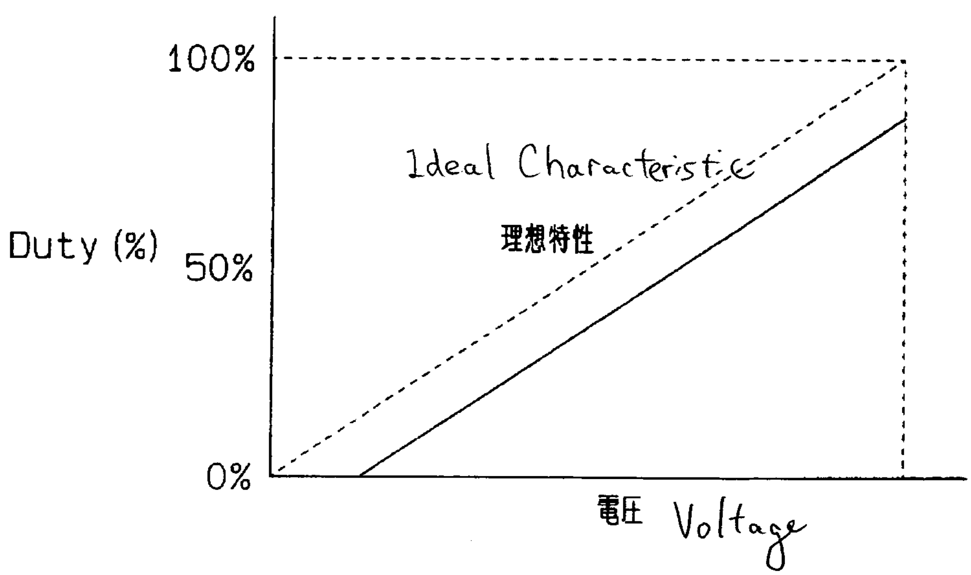
従来の休止期間設定回路の動作波形図



【図１２】[Fig.12]

ON Duty Characteristic Diagram

オン・デューティ特性の説明図



[Title of the Document] Abstract

[Abstract]

[Object] Providing a control circuit for a DC/DC converter that improves the ON duty characteristics of a main switching element.

[Means for Solving the Problems] An error amplification circuit 11 compares an output voltage Vo and a reference voltage Vr to output an error signal S1. A PWM comparison circuit performs pulse modulation based on the error signal S1 and the triangular wave signal S2 to generate a pulse signal S3. An idle period setting circuit 34 delays the pulse signal and generates a first control signal S14 having a pulse width that is the same as that of the pulse signal S3. A first drive signal SG11 provided to the main switching element 3 is generated based on the first control signal S14.

[Selected Drawing] Fig. 1